Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A switch comprising:~~Switch Comprising~~

a first transistor with main electrodes constituting in/outputs of the switch and with a control electrode constituting a first control input of the switch for in response to a first control signal controlling the first transistor;

a second transistor with main electrodes constituting the in/outputs of the switch and with a control electrode constituting a second control input of the switch for in response to a second control signal controlling the second transistor; and

a circuit for in response to the first control signal and an in/output signal at an in/output of the switch generating the second control signal, wherein the circuit comprises a generator for, in an enable mode with the first control signal having a first value, generating the second control signal having a second value;

wherein the generator comprises a third and a fourth transistor of which first main electrodes are coupled to each other and second main electrodes are coupled to each other, which first main electrodes are further coupled to a first main electrode of a fifth transistor which second main electrodes are further coupled to first main electrodes of a sixth seventh and eighth transistor for generating the second control signal with a control electrode of the third transistor being coupled to first main electrodes of a ninth and a tenth transistor, with second main electrodes of the seventh eighth and tenth transistor being coupled to each other, with a control electrode of the seventh transistor being coupled to the first main electrode of the seventh transistor and with control electrodes of the fifth sixth ninth and tenth transistor receiving the first control signal or a derived version thereof.

2. (canceled)

3. (currently amended) The switch ~~Switch~~ as defined in claim 1 ~~2~~, wherein the circuit further comprises

a detector for, in a disable mode with the first control signal having the second value, supplying the in/output signal to the generator for generating the second control signal having the first value in case of a value of the in/output signal being smaller than the first value and having the value of the in/output signal in case of the value of the in/output signal being larger than the first value.

4. (currently amended) The switch ~~Switch~~ as defined in claim 1, further comprising

a further circuit for in response to the first control signal and an in/output signal at an in/output of the switch generating a backgate signal destined for the second transistor.

5. (currently amended) The switch ~~Switch~~ as defined in claim 4, wherein the further circuit comprises

a further generator for, in an enable mode with the first control signal having a first value, generating the backgate signal having a value of the in/output signal and for, in a disable mode with the first control signal having a second value, generating the backgate signal having the first value in case of a value of the in/output signal being smaller than the first value and having the value of the in/output signal in case of the value of the in/output signal being larger than the first value.

6. (canceled)

7. (currently amended) The switch ~~Switch~~ as defined in claim 1 ~~6~~, wherein a detector comprises an eleventh and a twelfth transistor of which first main electrodes are coupled to each other for receiving the in/output signal or a derived version thereof, with a second main electrode of the eleventh transistor being coupled to a control electrode of the twelfth transistor and to a first main electrode of a thirteenth transistor with a second main electrode of the twelfth transistor being coupled to a control electrode of the eleventh transistor and to a first main electrode of a fourteenth transistor and to the second main electrodes of the seventh eighth and tenth transistor, with control electrodes of the thirteenth and fourteenth transistor receiving the first control signal or a derived version thereof.

8. (currently amended) The switch ~~Switch~~ as defined in claim 1 ~~7~~, wherein a further

generator comprises a fifteenth and a sixteenth transistor of which first main electrodes are coupled to each other for receiving the in/output signal or a derived version thereof and second main electrodes are coupled to each other and to a first main electrode of a seventeenth transistor for generating a backgate signal with a second main electrode of the seventeenth transistor being coupled to a first main electrode of an eighteenth transistor with control electrodes of the fifteenth sixteenth and seventeenth transistor receiving the first control signal or a derived version thereof, and with a control electrode of the eighteenth transistor receiving the in/output signal or a derived version thereof.

9. (currently amended) The switch ~~Switch~~ as defined in claim 8, wherein the second transistor is a PMOS having a backgate for receiving the backgate signal with the third transistor being a PMOS having a backgate coupled to its second main electrode, with the seventh and eighth transistor each being a PMOS having a backgate coupled to its first main electrode, with the tenth transistor being a PMOS having a backgate coupled to its first second electrode, with the eleventh and twelfth transistor each being a PMOS having a backgate coupled to its first main electrode, with the fifteenth and seventeenth transistor each being a PMOS having a backgate coupled to its second main electrode, with the eighteenth transistor being a PMOS having a backgate coupled to its first main electrode, and with all other transistors each being a NMOS.

10. (currently amended) An apparatus ~~Apparatus~~ comprising a switch as defined in claim 1; and further comprising a first stage coupled to a first in/output of the switch and a second stage coupled to a second in/output of the switch.

11. (new) A switch comprising:

a first transistor with main electrodes constituting in/outputs of the switch and with a control electrode constituting a first control input of the switch for in response to a first control signal controlling the first transistor;

a second transistor with main electrodes constituting the in/outputs of the switch and with a control electrode constituting a second control input of the switch for in response to a second control signal controlling the second transistor; and

a circuit for in response to the first control signal and an in/output signal at an in/output of the switch generating the second control signal, wherein the circuit comprises a generator for, in an enable mode with the first control signal having a first value, generating the second control signal having a second value;

wherein the generator comprises a third and a fourth transistor of which first main electrodes are coupled to each other and second main electrodes are coupled to each other, which first main electrodes are further coupled to a first main electrode of a fifth transistor for generating the second control signal.

12. (new) The switch as defined in claim 11, wherein the circuit further comprises

a detector for, in a disable mode with the first control signal having the second value, supplying the in/output signal to the generator for generating the second control signal having the first value in case of a value of the in/output signal being smaller than the first value and having the value of the in/output signal in case of the value of the in/output signal being larger than the first value.

13. (new) The switch as defined in claim 11, further comprising

a further circuit for in response to the first control signal and an in/output signal at an in/output of the switch generating a backgate signal destined for the second transistor.

14. (new) The switch as defined in claim 13, wherein the further circuit comprises

a further generator for, in an enable mode with the first control signal having a first value, generating the backgate signal having a value of the in/output signal and for, in a disable mode with the first control signal having a second value, generating the backgate signal having the first value in case of a value of the in/output signal being smaller than the first value and having the value of the in/output signal in case of the value of the in/output signal being larger than the first value.

15. (new) The switch as defined in claim 11, wherein a detector comprises an eleventh and a twelfth transistor of which first main electrodes are coupled to each other for receiving the in/output signal or a derived version thereof, with a second main electrode of the eleventh transistor being coupled to a control electrode of the twelfth transistor and to a first main electrode of a thirteenth transistor with a second main

electrode of the twelfth transistor being coupled to a control electrode of the eleventh transistor and to a first main electrode of a fourteenth transistor and to the second main electrodes of the seventh eighth and tenth transistor, with control electrodes of the thirteenth and fourteenth transistor receiving the first control signal or a derived version thereof.

16. (new) The switch as defined in claim 11, wherein a further generator comprises a fifteenth and a sixteenth transistor of which first main electrodes are coupled to each other for receiving the in/output signal or a derived version thereof and second main electrodes are coupled to each other and to a first main electrode of a seventeenth transistor for generating a backgate signal with a second main electrode of the seventeenth transistor being coupled to a first main electrode of an eighteenth transistor with control electrodes of the fifteenth sixteenth and seventeenth transistor receiving the first control signal or a derived version thereof, and with a control electrode of the eighteenth transistor receiving the in/output signal or a derived version thereof.

17. (new) The switch as defined in claim 16, wherein the second transistor is a PMOS having a backgate for receiving the backgate signal with the third transistor being a PMOS having a backgate coupled to its second main electrode, with the seventh and eighth transistor each being a PMOS having a backgate coupled to its first main electrode, with the tenth transistor being a PMOS having a backgate coupled to its first second electrode, with the eleventh and twelfth transistor each being a PMOS having a backgate coupled to its first main electrode, with the fifteenth and seventeenth transistor each being a PMOS having a backgate coupled to its second main electrode, with the eighteenth transistor being a PMOS having a backgate coupled to its first main electrode, and with all other transistors each being a NMOS.

18. (new) An apparatus comprising a switch as defined in claim 11; and further comprising a first stage coupled to a first in/output of the switch and a second stage coupled to a second in/output of the switch.